



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,010	02/27/2002	Thomas E. Willis	ITL.0630P1US (P12054X)	4222
21906	7590	10/09/2007	EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			ABDULSELAM, ABBAS I	
		ART UNIT	PAPER NUMBER	
		2629		
		MAIL DATE	DELIVERY MODE	
		10/09/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/086,010	WILLIS, THOMAS E.
	<b>Examiner</b>	<b>Art Unit</b>
	Abbas I. Abdulselam	2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 24 August 2007.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-8, 10, 12-19, 21-23, 25-27, 34 and 44-54 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 21-23, 25-27, 34, 46, 47, 50 and 53 is/are allowed.

6) Claim(s) 1, 2, 3, 10, 12-18, 44, 45, 48, 49, 51, 52 and 54 is/are rejected.

7) Claim(s) 4-8 and 19 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____ .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

1. This office action is in response to a communication filed on August 24, 2007. Claims 1-8, 10, 12-19, 21-23, 25-27, 34 and 44-54 are pending.

### **Rejections under 35 U.S.C. 112 first paragraph**

2. In view of the argument filed on August 24, 2007, rejections under 35 U.S.C. 112 first paragraph is withdrawn.

### *Response to Arguments*

3. Applicant's arguments filed August 24, 2007 have been fully considered but they are not persuasive.

Applicant argues that independent claims 1 and 15 as amended have limitations, a multi-pixel display array on a first die and multi-pixel memory array on a second die separate from the first die that are not taught by Numao (USPN 6937222).

However, as shown in the art rejection below, Numao teaches as shown in Fig. 30 a display section (310), a memory (308) such that image memory (308) is configured outside the display section (310).

Furthermore, it is known as pointed out by Numao that locating the memory outside the display region requires an additional area on the display substrate, which means a smaller number of substrates fabricated from a glass substrate (of an equal display area) in a TFT process (col. 4, lines 64-67 and col. 5, lines 1-5) Hence, the claim limitations "a first die, second die, a second die being separate from the first die" are taught and covered by Numao' background teachings.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 10, 15, 44-45, 48-49, 51 and 54 are rejected under 35 U.S.C. 102(e) as being anticipated by Numao (USPN 6937222).

Regarding claims 1, 15 and 48, Numao (USPN 6937222) teaches a spatial light modulator (Fig. 30 (LCD)) comprising: a multi-pixel display array on a first die; (Fig. 30 (310), display section, col. 4. lines 64-67 and col. 5, lines 1-5) and a multi-pixel memory array on a second die separate from the first die the multi-pixel memory array having pixel storage cells; (Fig. 30 (308), memory, col. 4. lines 64-67 and col. 5, lines 1-5) wherein at least some pixels of the multi-pixel memory array are disposed outside the multi-pixel display array such that the multi-pixel memory array is physically decoupled from the multi-pixel display array (see fig. 30, col. 4, lines 10-15, outside display section 310, image memory 308 is configured).

Regarding claims 2, and 51, Numao teaches all of the pixels of the memory array are disposed outside the display array ((col. 4, lines 10-15, outside display section 310, image memory 308 is configured).

Regarding claims 10, 44-45 and 49, Numao teaches a spatial light modulator (Fig. 30 (LCD)) comprising: control logic; (Fig 30 (305), address line converter circuit) a pixel memory array coupled to the control logic and occupying a first area of the spatial light modulator; (Fig. 30 (305,308)) and a pixel display array coupled to the control logic and the pixel memory array, and occupying a second area of the spatial light modulator (Fig. 30 (310, 308, 305), wherein the first and second areas are physically decoupled and substantially non-overlapping, the pixel display array comprising a plurality of pixel display cells, each having disposed within its area an associated pulse width modulation drive circuit (see fig. 30, col. 4, lines 10-15, outside display section 310, image memory 308 is configured).

Regarding claim 54, Numao teaches the first die is formed using a first semiconductor technology and the second die is formed using a second a semiconductor technology (col. 4. lines 64-67 and col. 5, lines 1-5).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3, 12-14, 16-18 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Numao (USPN 6937222) in view of Mitsuo et al. (JP 2000-098954).

Regarding claims 3 and 16-18, Numao does not teach at least one local pulse width modulation drive circuit coupled to at least one of the pixel storage cells and a global counter coupled to the local pulse width modulation drive circuit.

Mitsuo on the other hand teaches a control circuit, which includes a PWM frequency setting register, (30) and a frequency counter (32) outputting a clock in which a clock is counted with respect to a value of the PWM frequency setting register (Drawing 2 (30, 32), [0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numao's Liquid crystal display shown in Fig. 30 to adapt Mitsuo PWM frequency setting register, (30) and a frequency counter (32) as configured in drawing 2 because the use of PWM frequency setting register, (30) and a frequency counter (32) is such that they form as integral components of a liquid crystal controller (12) as taught by Mitsuo ([0031], [0033]).

Regarding claim 52, While Numao teaches the pixel display array comprises a plurality of pixel display cells, (Fig. 30 (310)) and the pixel memory array comprises a plurality of pixel memory cells (Fig. 30 (308)).

Numao does not teach a plurality of display cells each having disposed within its area an associated pulse width modulation driver circuit.

Mitsuo on the other hand teaches a control circuit, which includes a PWM frequency setting register, (30) and a frequency counter (32) outputting a clock in which a clock is counted with respect to a value of the PWM frequency setting register (Drawing 2 (30, 32), [0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Numao's Liquid crystal display shown in Fig. 30 to adapt Mitsuo PWM frequency setting register, (30) and a frequency counter (32) as configured in drawing 2 because the use of PWM frequency setting register, (30) and a frequency counter (32) is such that they form as integral components of a liquid crystal controller (12) as taught by Mitsuo ([0031], [0033]).

Regarding claim 12, Mitsuo teaches the control logic comprises a counter for providing a count value; the pulse width modulation driver circuit comprises a comparator coupled to compare the count value to a pixel value stored in an associated pixel array cell of the pixel memory array (PWM frequency setting register, (30) a frequency counter (32) and a duty counter 33, Drawing 2 (30, 32), [0033]).

Regarding claim 13, Mitsuo teaches means to provide non-linearity in the pulse width modulation (PWM frequency setting register, (30), PWM duty setting register (31), Drawing 2 (30, 31), [0033]).

Art Unit: 2629

Regarding claim 14, Numao teaches the pixel memory array comprises: more memory cells than the pixel display array has pixel display cells; and means for providing redundancy in the pixel memory array (Fig. 30 (311,312), memory line selector circuit 311, display line selector circuit 312).

*Allowable Subject Matter*

8. Claims 21-23, 25-27, 34, 46-47, 50 and 53 are allowed
9. Claims 4-8 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2629

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas abdulselam

Examiner

Art Unit 2629



RICHARD HJERPE  
SUPERVISORY PATENT EXAMINER  
TECHM 2600